Amendments to the Specification:

Please replace the paragraph on page 13, starting at line 8, with the following amended paragraph:

The power module PA-MDL comprises the power amplifier 200, a voltage control circuit for generating a drive voltage (Vdd) of the above-mentioned power amplifier 200, the output detecting means 201, and the like. The power amplifier 200 is configured with a FET or the like. The drive voltage (Vdd) corresponding to a control voltage VAPC supplied from the amplitude loop of the above-mentioned high frequency IC 100, by the voltage control circuit provided in the power module PA-MDL, is generated and applied to a drain terminal or a source terminal of this FET. Further, an ~~appreciate~~appropriate bias voltage VBIAS generated in a bias circuit (not shown) is applied to a gate terminal of the power FET (200). The output detecting means 201 is configured by signal branching means comprising a coupler formed on a module substrate, or a capacitor for branching and propagating only an alternating component of an output, or the like.

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Please replace the paragraph bridging pages ~~13 and 14~~ 13, 14 and 15, starting at line 25, with the following amended paragraph:

The high frequency IC 100 is configured by a phase frequency divider 110 for generating signals whose phases are shifted 90 degrees with respect to each other, from an oscillation signal ϕIF of an intermediate frequency generated in an oscillator IF-VCO; a quadrature modulator 120 for mixing an I and Q signals supplied from the base band LSI 300 and the ~~signals~~ frequency-divided signals in the phase frequency divider 110 to perform a quadrature modulation; a phase detector 240 for detecting the phase difference between a feedback signal from the above-mentioned